Abstract of the Disclosure:

A method and a device for reducing addresses of faulty memory cells compare addresses of faulty memory cells, as first fault addresses, with addresses of word lines or bit lines which are to be completely repaired, these addresses are referred to as second fault addresses. If the first fault address corresponds to the second fault address, the first fault address is deleted and not further processed. In a second comparison, it is determined, by reference to the number of non-deleted first fault addresses, whether an address of a word line or bit line is used as a new second fault address for the first comparison method. The number of addresses of faulty memory cells are thus reduced.

MB/vs